MBI6030 Application Note

Foreword

The MBI6030 is an LED constant current driver for RGB cluster application. The stability of data transmission is improved through clock re-generation and A-token. This article consists five chapter; the chapter 1 is the module design, including the notices of VDDH, CA, LED... etc. The chapter 2 is the controller design, including notice for controller, CKI frequency... etc. The chapter 3 is the production and setup, including realize the effect of hot swap, the connector design of how to reduce the surge voltage when clusters are installed or removed, the procedures of production…etc. The chapter 4 is the method of system testing. And the last chapter is other applications notice, such as long power of PCB.

Chapter 1. Module Design

Figure 1 is the application circuit of MBI6030.

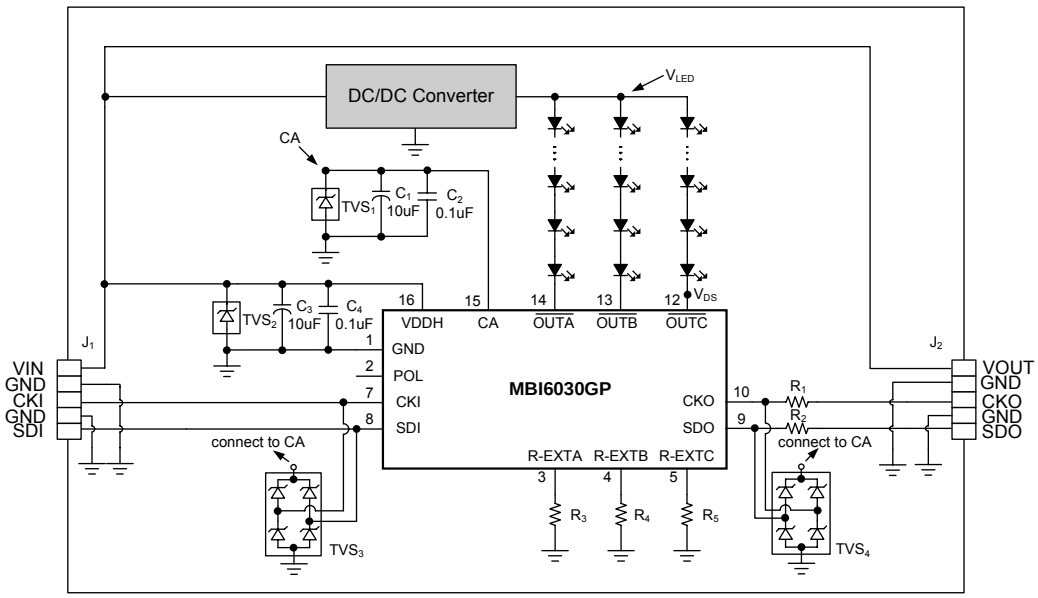

Figure 1. MBI6030 application circuit

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1. VDDH and CA Precautions

In order to steady IC, **user shouldn't connect CA to other device, such as LED, buffer (ex. 74HC244)**, and add capacitance on CA, as shown in Figure 2.

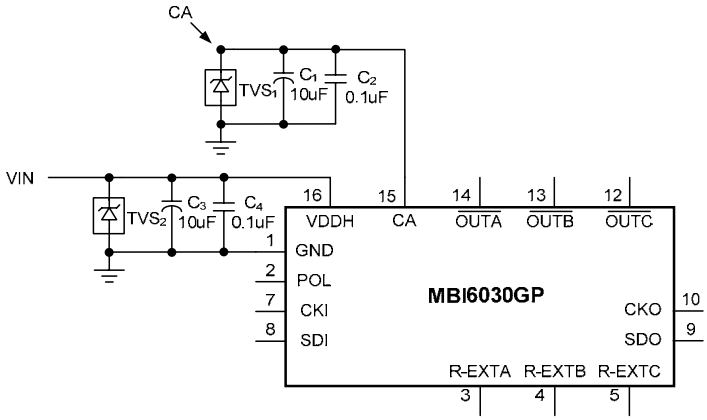

Figure 2. the sketch map of power

2. LED Notice

A large V_{LED} may result in high voltage drop on MBI6030's output port while adopting LEDs with large variation of forward voltage and then the MBI6030 will have overheat problem. Therefore, LED forward voltage (V_F) sorting is necessary.

3. Setting Current Notice

The MBI6030 allows users to set the three LED current (I_{OUT}) by an external resistor, R_3~R_5. After users decide the LED current, users can get a suitable R_3~R_5 by the following equations

$$R_3 \sim R_5 = (0.41V / I_{OUT}) \quad \text{..... (1)}$$

R_3~R_5 must be placed close to MBI6030 in order to prevent R_3~R_5 from being disturbed. Moreover, the resistor with 1% tolerance is recommended to enhance the output current accuracy.

To keep the MBI6030 constant current, a sufficient voltage at $\overline{OUTA}$, $\overline{OUTB}$ and $\overline{OUTC}$ of IC (V_{DS}) is needed. Figure 3 shows the I-V curves of MBI6030. Users can refer to the Figures 3 and get a suitable V_{DS}. In general, the V_{DS} is slightly greater than the knee voltage. (Recommendation: V_{DS} = V_{knee}+0.2V)

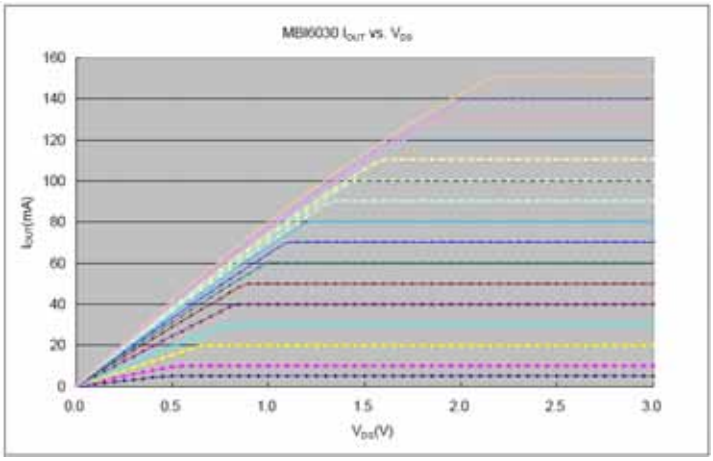

Figure 3. The I-V curves of MBI6030

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4. LED Power Determined

As shown in Figure 4, the minimum $V_{LED, MIN.}$ can be determined by the following equation

$$V_{LED, MIN.} = (V_{F, MAX.} \times n) + V_{DS} \quad \text{..... (2)}$$

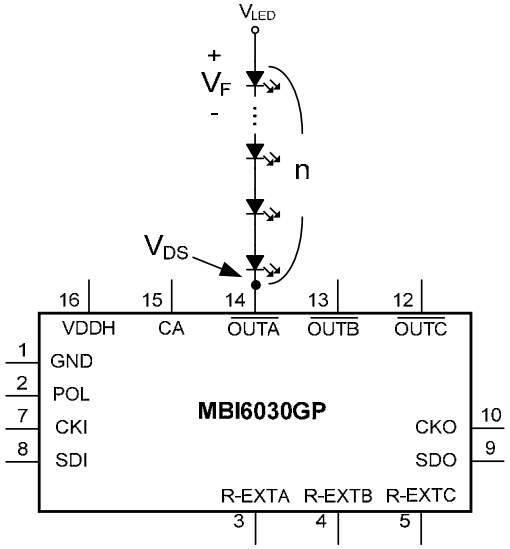

Figure 4. The sketch of minimum V_{LED} voltage

where $V_{F,MAX}$ represents the maximum forward voltage of LED, and n is the number of cascaded LEDs. The maximum sustaining voltage of $\overline{OUTA}$~$\overline{OUTC}$ is 40V. If the supply voltage of LED (V_{LED}) is over 40V, the IC will be damaged.

5. Power Configure

Because of the impedance of power lines, the voltage of each cluster might be different in the multi-cluster cascaded application as shown in Figure 5. Users have to calculate the dropout voltage caused by the impedance of power line. For example, the maximum conductor impedance of AWG26 (Maximum Conductor Resistance) of UL1007 is 152Ω/km. It means that 1km transmission line is equal to 150Ω. If transmission line is 50cm and current is 20mA, there will be 1.52mV voltage drop. If the voltage is lower than that of DC/DC converter supply voltage, users should use a new power line, as shown in Figure 8.

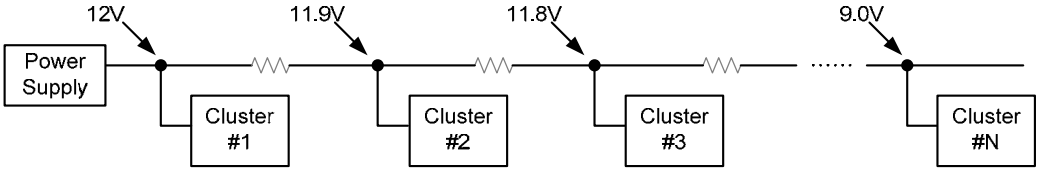

Figure 5. The sketch of dropout voltage in multi-cluster cascaded application

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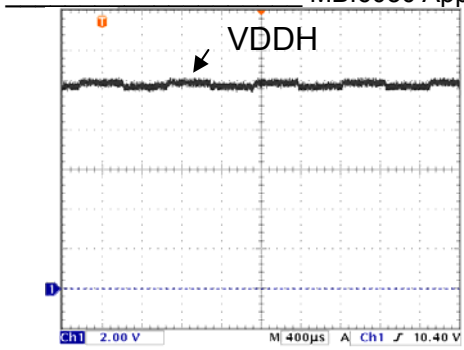

Figure 6. The poor waveform of power

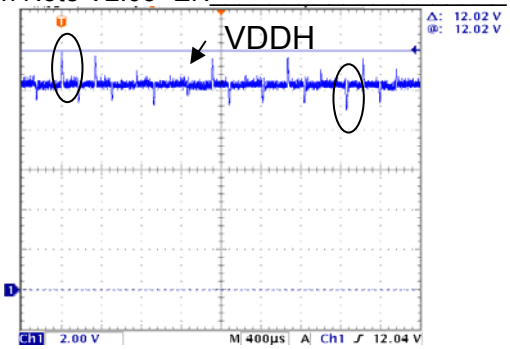

Figure 7. The poor waveform of power

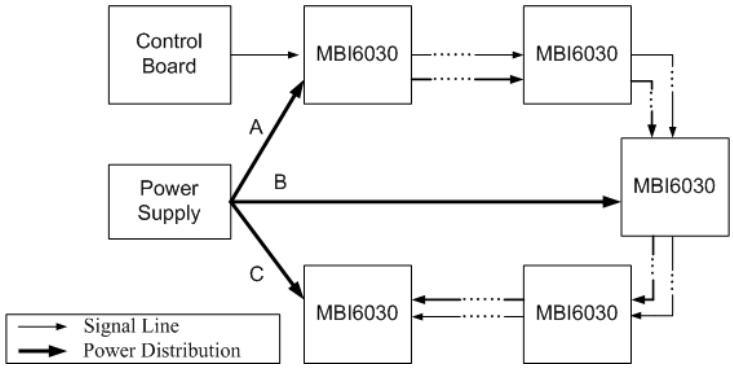

Figure 8. The power distribution of clusters

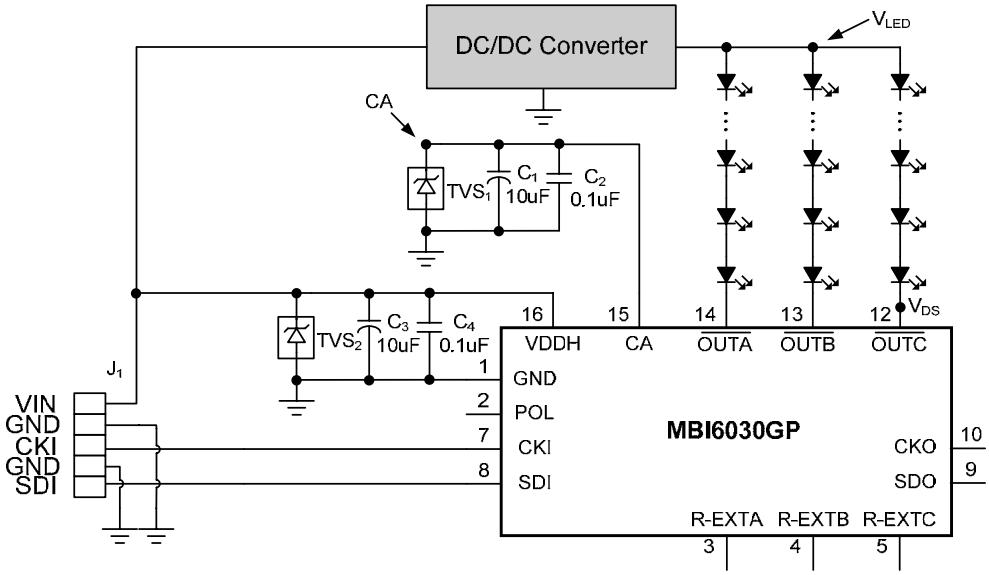

Figure 9. Use the sketch map of DC/DC converter

Table 1. The specification of transmission line

UL 1007 / CSA TR-64	Range		Conductor		Insulation		Tolerance mm	Maximum Conductor Resistance Ω/km	Permitable Current A	Minimum Insulation Resistance MΩ/km	Insulation Potential Strength VAC/min
	Temp ℃	Voltage V	AWG	NO./MM	Thickness mm	O.D. mm					
Stranded	UL 80℃ CSA 90℃	300V	32	7/0.080	0.38	1.00	±0.10	703	1.6	15	2000
			30	7/0.100	0.38	1.10	±0.10	397	2.0		
			28	7/0.127	0.38	1.20	±0.10	248	2.5		
			26	7/0.160	0.38	1.30	±0.10	152	3.5		
			24	11/0.160	0.38	1.45	±0.10	88.6	5.0		
			22	17/0.160	0.38	1.60	±0.10	62.5	7.0		
			20	21/0.180	0.38	1.85	±0.10	39.5	9.0		
			18	34/0.180	0.38	2.10	±0.10	24.4	13.0		
			16	26/0.254	0.38	2.40	±0.10	15.6	17.0		
Top-Coated(ATC)			30	7/0.100	0.38	1.10	±0.10	397	2.0		
			28	7/0.127	0.38	1.20	±0.10	248.0	2.5		
			26	7/0.160	0.38	1.30	±0.10	152.0	4.0		
			24	7/0.200	0.38	1.45	±0.10	88.6	5.3		
			22	7/0.254	0.38	1.60	±0.10	62.5	7.2		
Solid(TA)			26	1/0.404	0.38	1.25	±0.10	155	3.8		
			24	1/0.511	0.38	1.40	±0.10	92.4	5.3		
			22	1/0.643	0.38	1.55	±0.10	60.1	7.2		
			20	1/0.813	0.38	1.70	±0.10	37.0	9.4		
			18	1/1.020	0.38	1.96	±0.10	23.6	13.0		

6. Signal Quality Notice

Good waveform quality should be no crosstalk , no overshoot/undershoot and the amplitude of the voltage is higher than V_{IH}. Figure 10 describes the signal waveform with good quality.

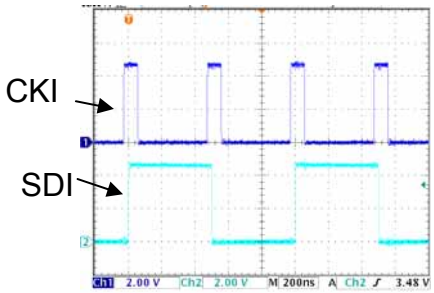

Figure 10. Good quality signal waveform

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6.1 Cross-talk

When two signal lines are juxtaposed together, a cross-talk phenomenon will happen on these two signals, as shown in Figure 11. In order to suppress this phenomenon, a GND line to separate these two signals is necessary, as shown in Figure 12. A twist pair cable is easy to suffer cross-talk phenomenon; therefore, we do not suggest adopting the twin wire in this application.

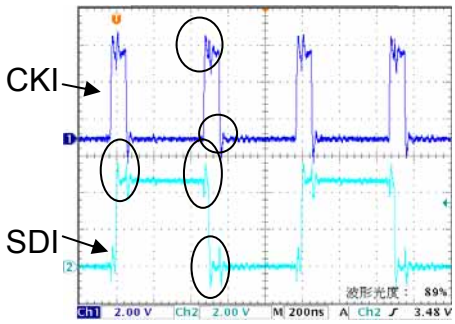

Figure 11. The waveform of cross-talk

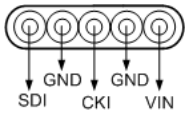

Figure 12. The arrangement of transmission line

In order to reduce the noise interference, the cable wire with shield is recommended to be the transmission line; also, the braid and drain wire of foil must connect to ground.

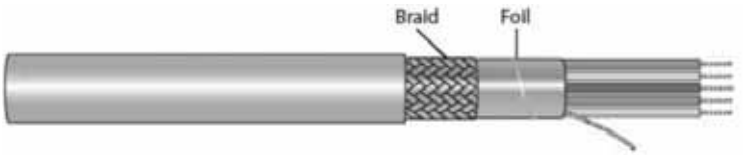

Figure 13. The cable wire with shield

6.2 Overshoot / Undershoot Voltage

Figure 14 shows the overshoot and undershoot voltage on CKI and SDI signals. In order to improve the signal quality, reserved the PCB positions of R_1 and R_2 in Figure 15 are recommended. The resistances of R_1 and R_2 will affect the rising and falling time of CKO/SKO, the larger resistance results the slower rising/falling time and reduce the effect of over/under shoot voltage. However, the large resistance might cause abnormal transmission.

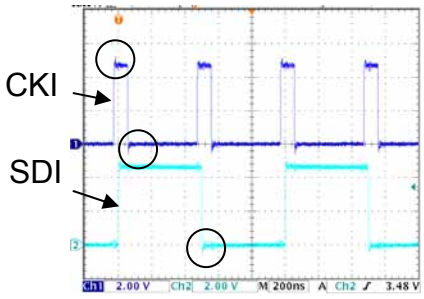

Figure 14. The poor waveform of overshoot or undershoot voltage

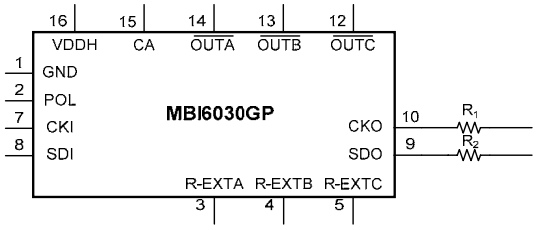

Figure 15. The sketch of how to improve the poor waveform

6.3 Amplitude

The factors affecting amplitude include equivalent capacitance of wire, equivalent capacitance of TVS, and resistance of CKO/SDO. User can choose shorter wire to reduce the equivalent capacitance and smaller equivalent capacitance of TVS and adjust resistance of CKO/SDO.

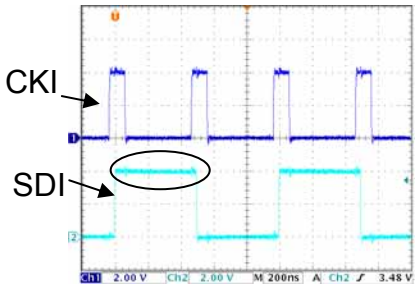

Figure 16. The poor waveform of insufficient amplitude

7. Notice About Test Pin

The pin 6,11 of GP package and pin 2,3,4,5,11,14,15,16,17,20 of GFN package are test pins. Please not connect these pins to avoid IC into test mode.

Chapter 2. Control Signal Design

1. Notice for Controller

In order to improve the validity of controller signal, the controller signal should wait steady power, and use power-on reset circuit to reset the system. The CKI and SDI of controller should use GND shielding and the controller must add a GND as common GND for the module.

2. CKI frequency Notice

The minimum CKI frequency of MBI6030 is 80kHz. Users should use fixed CKI frequency to improve system stability.

3. Time-out Protection

The time-out protection of MBI6030 is used to ensure the data count. It uses the internal counter to calculate the stop period of CKI. When the CKI stop time exceeds 23 CKI, MBI6030 will ignore the present input data and keep the previous input data until the next input data is correctly recognized.

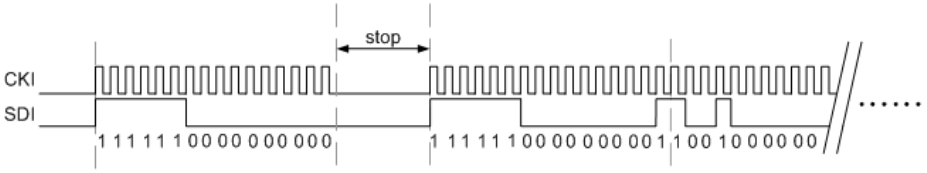

Figure 17. Diagram of time-out

4. Input Signal

The output signal of controller should allow the falling edge of CKI in the middle of SDI data. The recommended CKI is 50% of the duty, as shown in Figure 18.

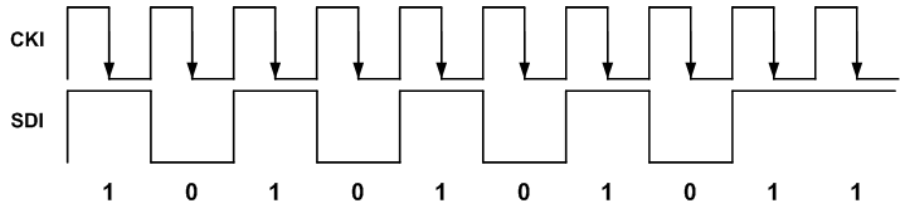

Figure 18. The falling edge of CKI in the middle of SDI data

The input signals must include the prefix, header and the data.

Prefix	Header	Data

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4.1 Prefix

The prefix is the time that the CKI and SDI pull low (T_{d0}) simultaneously. In order to make MBI6030 realize the new gray scale and meet the image refresh time (T_{frame}), the following equations can be used to calculate the prefix.

$$T_{d0} \leqq T_{frame} - T_{Data} \quad \text{.....(3)}$$

$$T_{d0} > 44 \times \text{CKI cycle} \quad \text{.....(4)}$$

where T_{Data} represents the time of transmission data, 16-bits $T_{Data} = T_{CKI} \times 48 \times (N+1)$ and 10-bits $T_{CKI} \times 30 \times (N+1)$, N is the series IC count, T_{CKI} is the CKI period.

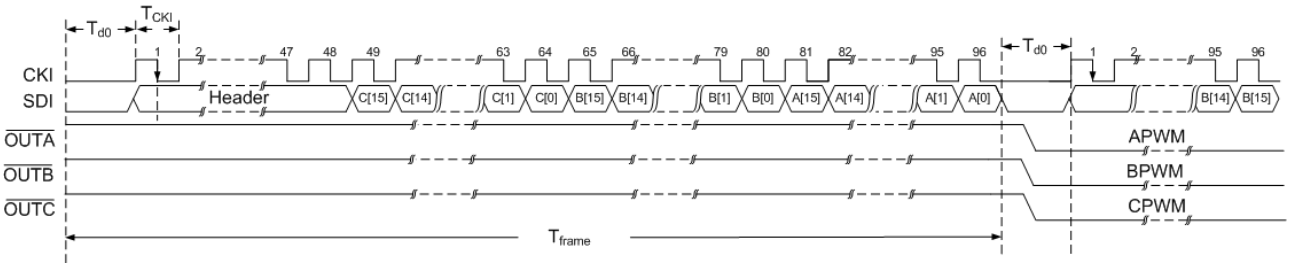

Figure 19. Diagram of prefix

Example

Number of MBI6030 in cascade: 256 pcs,

Gray scale data:16-bit,

Period of CKI (T_{CKI}): 1us (1/1MHz),

Refresh time of a frame: 16.67ms (1/60Hz).

From equation (3), T_{d0} = 16.67ms –1us x 48 x (256+1) = 4.33ms. The time is much larger than the time of 44-CKI (44×1us=44us). The data stream can be recognized, as shown in Figure 20.

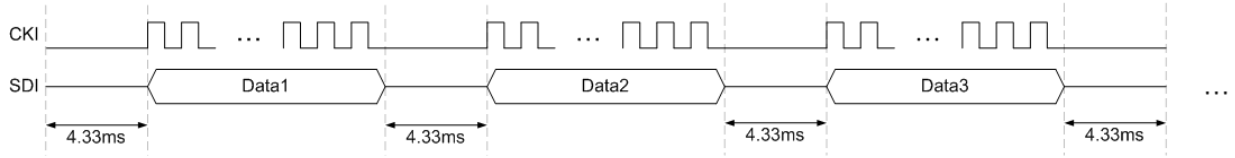

Figure 20. The Diagram of prefix is 4.33ms

4. 2 Header

The correct Header must be transmitted before the gray scale data to make sure each MBI6030 can catch the gray scale data with correct address. The header includes H(Command Header),A(Address), L(Length) and P(Parity Check).

4.2.1 Command Header illustration

MBI6030 has six types of Command Headers, as shown in Table 2. According to the definition of each header, the consequent data will be written to gray scale data or dot correction data.

Table 2. Three kinds of command

Command H[5:0]	Data Type
6'b11 111s	16-bit gray scale data
6'b10 101s	10-bit gray scale data
6'b10 011s	6-bit dot correction data

bit "s": 1, high-frequency GCLK (9MHz±10%)

bit "s": 0, low-frequency GCLK (4.5MHz±10%)

4.2.2 The Illustration of Address and Length

The method of MBI6030 address setting is A-Token. The theorem of A-Token is to distribute the A(Address) and L(Length) to each IC automatically. The address data will add 1 whenever the data chain pass to the next IC, and the Least Significant Bit (LSB) will be exported first to address the next IC. When the data of address and length are the same, the data will be latched to register. **The length of MBI6030 is the amount of cascaded ICs minus one.** For example, if there are two MBI6030 in cascaded, the length will be 1(10'b0000000001), and **the initial address is 0(10b'0000000000).**

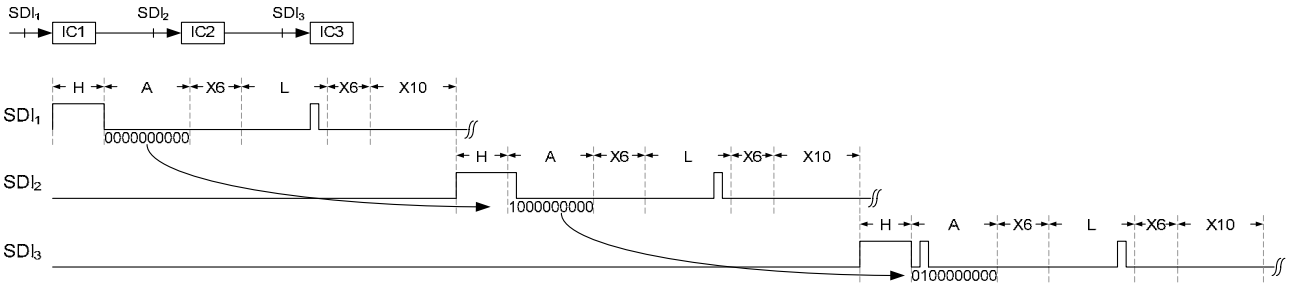

Figure 21. Diagram of A-Token

Following shows the example of two MBI6030 in cascade with different commands

6- bit Dot Correction Data

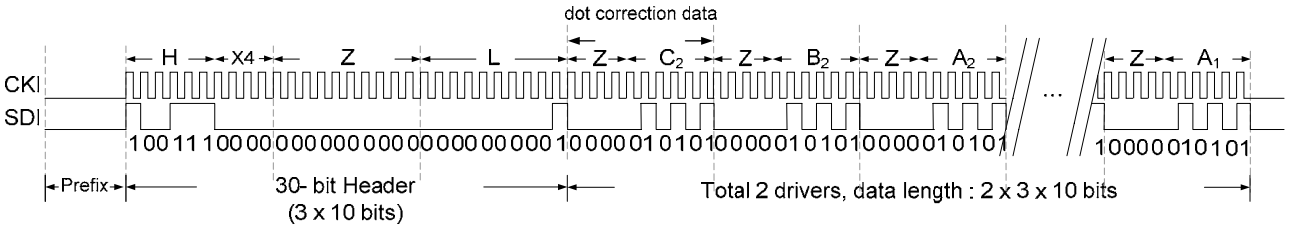

Figure 22. The example of 6-bit dot correction data

where two Command Headers must be filled with 6b'10011 in the Header. Every correction data only fill one time, such as ZC_2,ZB_2,… As the Length sets 1(10'b0000000001), it totally needs 2 x 3 x 10 bits of dot correction data after the Header.

10- bit Gray Scale Data

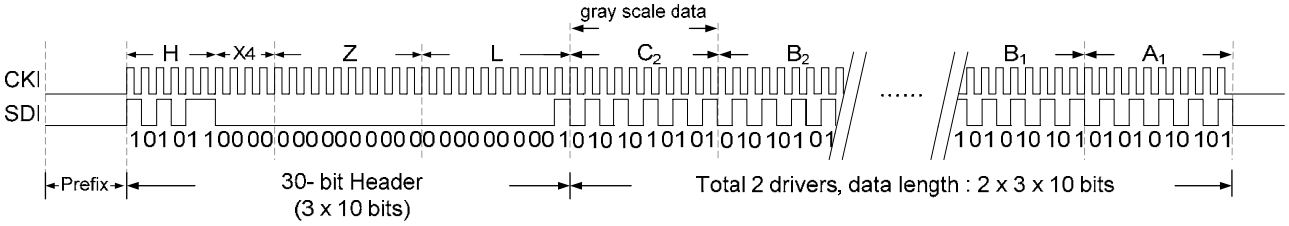

Figure 23. The example of 10-bit gray scale data

where two Command Header must be filled with 6b'101011 in the Header. As the Length sets 1(10'b0000000001), it needs 2 x 3 x 10 bits gray scale data after the Header.

16- bit Gray Scale Data

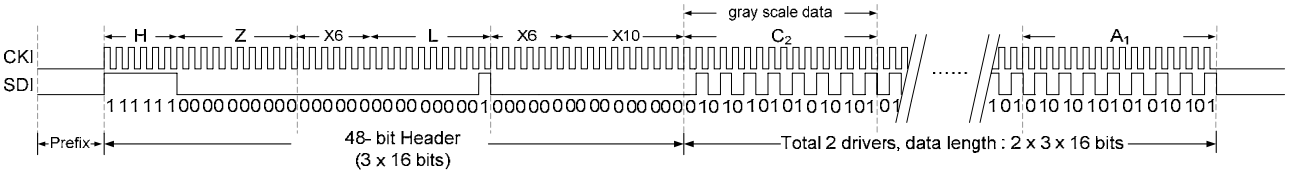

Figure 24. The example of 16-bit gray scale data

where two Command Header must be filled with 6b'111111 in the Header. As the Length sets 1(10'b0000000001), it needs 2 x 3 x 16 bits gray scale data after the Header.

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Chapter 3. Production and Setup

1. Realize the effect of hot swap

Hot swapping means the action of connecting or disconnecting the pin of VDDH/CKI/SDI/CKO/SDO in MBI6030 when in operation. It will induce the large instantaneous current and voltage, and then to damage the IC. Besides increasing the EOS protection component as mentioned, users also may use the longer ground terminal in connecters and operate the correct procedures to avoid hot swap.

2. Connecter Design to Reduce Strike Voltage

2.1 Resistance

Cascade a resistor at CKO and SDO can reduce the probability of IC been damaged by hot swap. The larger resistance results the lower probability of damage problem, and the lower speed of transmission. The recommended resistances of R_1 and R_2, which are shown in Figure 15, are 33Ω.

2.2 Connector

When setting up or removing the connecter of cluster instantly, in order to reduce the un-expected spike voltage and avoid IC burned out, users must turn off the power first, and then to set up or remove the cluster. It is better to connect GND first. The GND terminal should be designed longer than the VIN to reduce the unexpected strike voltage, the recommended design of power and signal connectors are shown as Figure 25 respectively.

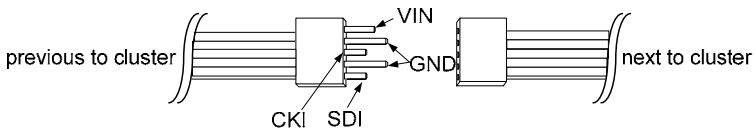

Figure 25. The safety design of longer terminal ground

2.3 Transient Voltage Suppressor

The products of Macroblock, Inc. have conformed to the standard of ESD protection. For enhancing Electrical Over Stress (EOS) protection, an external device, Transient Voltage Suppressor (TVS) diode is required, as shown in Figure 25. Followings show the guideline for TVS selection.

TVS_1:

a. The maximum Reverse Stand-Off Voltage (V_{RWM}) is required to be 5V.

b. The maximum clamping voltage (V_C) needs to be larger than 5V.

c. TVS diode should be placed to the protected pins as close as possible to prevent the EOS happened.

TVS_2:

a. The maximum Reverse Stand-Off Voltage (V_{RWM}) is required to be 30V.

b. The maximum clamping voltage (V_C) needs to be large than 30V.

c. TVS diode should be placed to the protected pins as close as possible to prevent the EOS happened.

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TVS_3 and TVS_4:

a. The maximum Reverse Stand-Off Voltage (V_{RWM}) is required to be 5V.

b. The maximum clamping voltage (V_C) needs to be large than 5V.

c. The parasitic capacitor of TVS will affect the rise/fall times of CKO/SDO, signal amplitude and transmission frequency.

d. TVS diode should be placed to the protected pins as close as possible to prevent the EOS happened.

e. The power of TVS must connect to CA. User must add TVS and capacitance on CA.

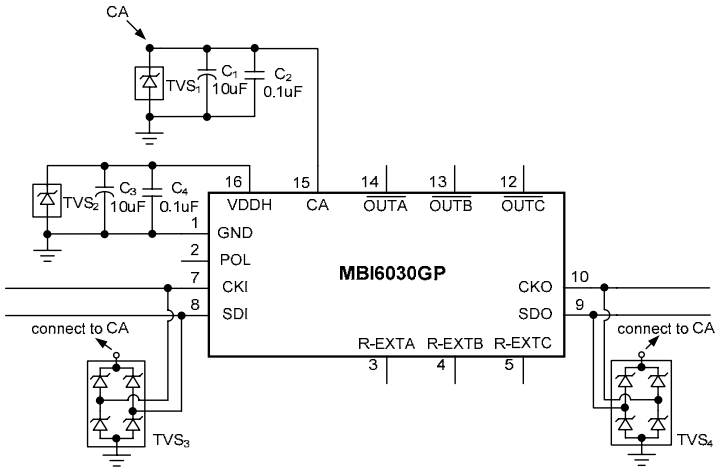

Figure 26. The component position of EOS

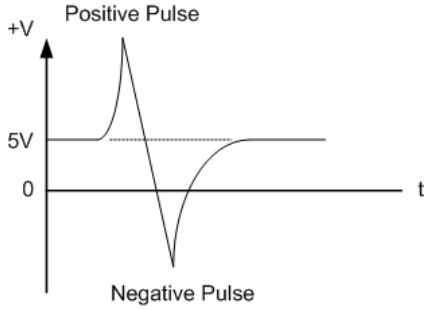

Figure 27. without use EOS component

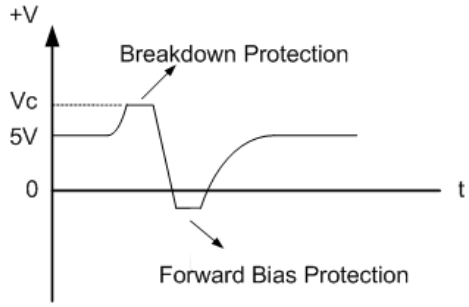

Figure 28. with use EOS component

3. Production and Setup procedures

The correct procedures to produce and setup the LED cluster are listed as below:

Step 1. Shut down the power system before setting up the LED cluster system.

Step 2. Before connecting the LED cluster system, the static electricity on clusters should be discharged.

Step 3. Make sure ground lines are connected well and correctly.

Step 4. Make sure all the wires, including power and signal transmission lines, have been connected well and correctly.

Step 5. After above steps, turn on the supply power.

Step 6. If users need to re-solder the device during removing module or production procedures, the power system should be shutdown. After the electric charge in the capacitance is discharged from the module, users can remove module or solder the device.

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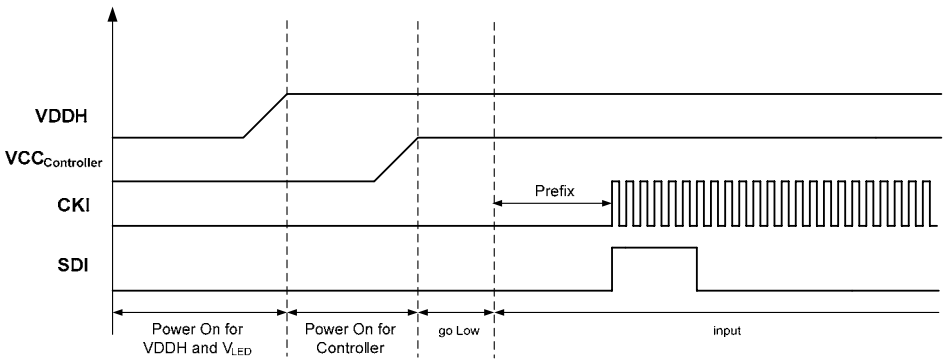

Figure 29. Power-on sequence

4. Printed Circuit Board Notice

1. Users should avoid the situation of empty solder, cold solder, and split solder in manufacturing process of printed circuit board (PCB)
2. Device layout should avoid to approach the board edge of PCB.
3. To design the longer size of PCB, we suggest to select the thick slab value of PCB to avoid soldering issues due to board bending.

Chapter4. The Method of System Testing

The CKI frequency needs to be adjusted by the signal quality and the amount of cascaded cluster. Users can follow the below steps to verify the system stability

Step1. Set the CKI frequency to 1MHz

Step2. Set the 16-bit gray scale to 0101010101010101 or 0101010101 for 10-bit.

Step3. Follow the sequence of R, G, B, R, G, … to light up LED.

Step4. If all the clusters work normally, the CKI frequency can be increased by 500kHz per step, until the cluster transmission is failed.

If the cluster transmission is failed at step 1, that means the system can not work at 1MHz CKI frequency. The CKI frequency can be decreased until 80kHz. If the system still can not work at 80kHz CKI frequency, please check the signal quality of CKI/SDI.

Chapter 5. Other application Notice

1. Using the long power line on the PCB

If users have to use the long power line on the PCB, the distribute capacitors, which as Figure 30 shows, are recommended. The value of C_d is depended on the distance between each Power Line.

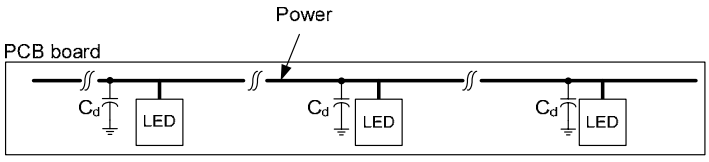

Figure 30. The sketch of distributed capacitance

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2. Logic Level Issue

As voltage drop effect, the CA of each cluster is different; it will lead to the different logic level between clusters, as shown in Figure 31. When CA is 5V, the V_{IH}/V_{IL} level will be 3.65V/1.4V respectively. And if the CA of another cluster is 4V, the logic level will be 2.92V/1.12V. The different logic level will cause a different trigger time and then impact the signal transmission. Please refer to the section of "Power Configure" for the suggested method.

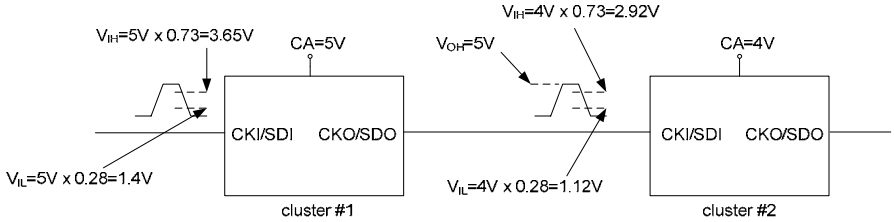

Figure 31. The diagram of different CA

Summary

In the application of multiple clusters cascaded, the following notices must be taken

1. The transmission line with small parasitic inductance is required to enhance the signal quality.
2. To prevent the insufficient V_{LED}, which is caused by the conductor resistance in transmission line, results the problem of cluster brightness unbalance, please refer Figure 8 to design the power source.
3. Please refer to chapter 3, “Production and Installation”, to protect IC being damaged from hot-plug in. Please take a note, even the processes in chapter 3 have been executed, it only can reduce the probability of burn-out when hot-plug in, can’t totally solve the problem.

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